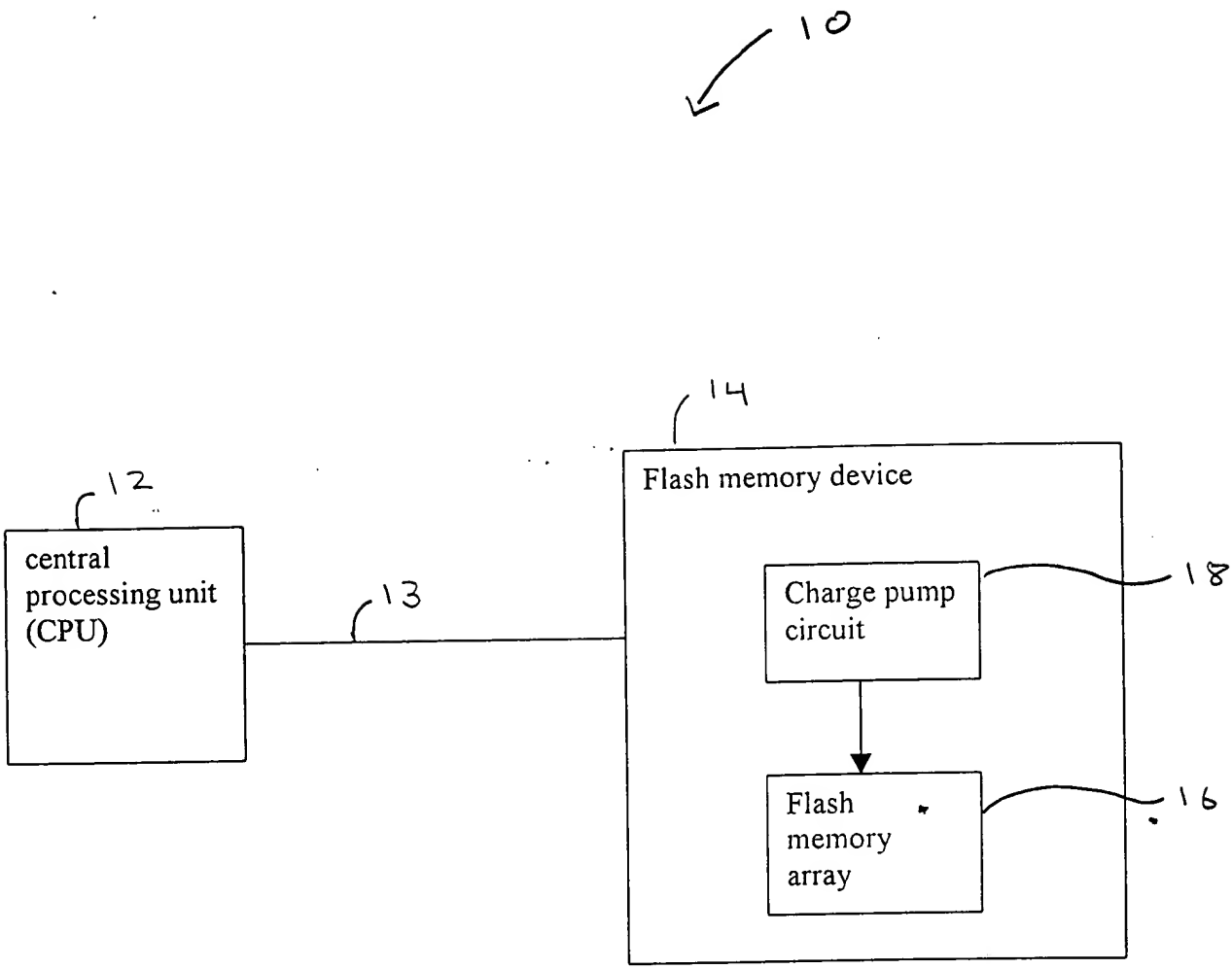
10
14
Flash memory device
12
central processing unit (CPU)
13
Charge pump circuit
18
Flash memory array
16

FIG. 1

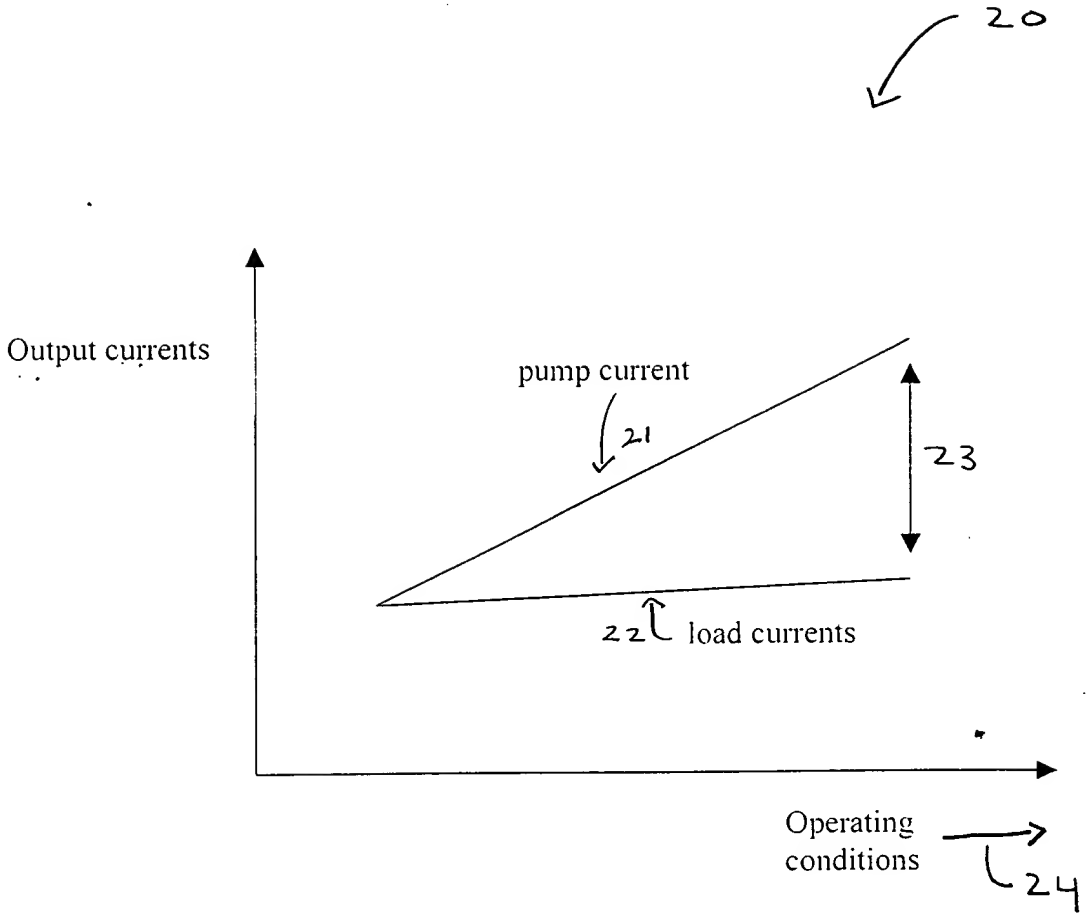
20
Output currents
pump current
21
23
22
load currents
Operating
conditions
24

FIG. 2

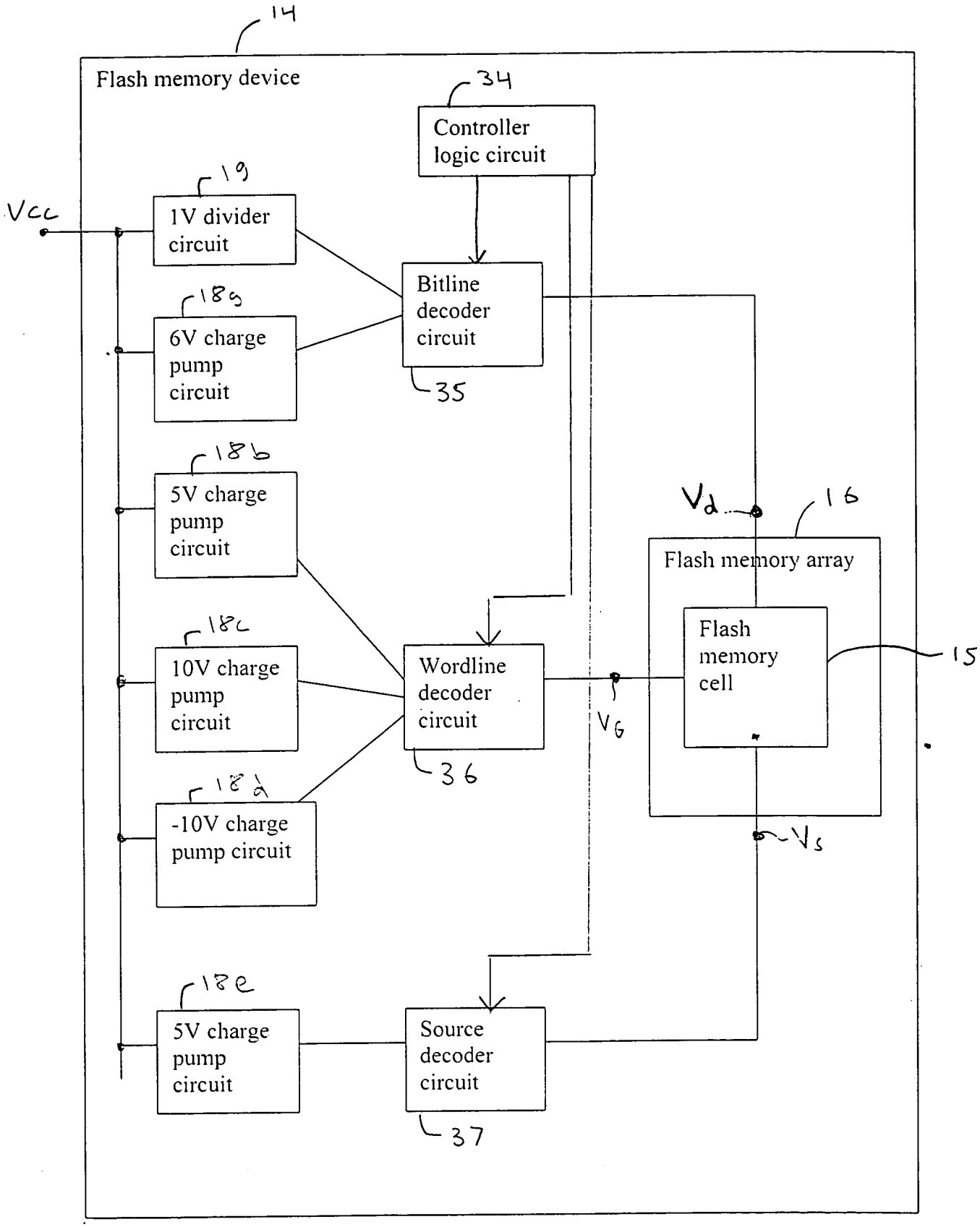
14
Flash memory device
34
Controller logic circuit
19
1V divider circuit
Vcc
18a
6V charge pump circuit
Bitline decoder circuit
35
18b
5V charge pump circuit
Vd
16
Flash memory array
18c
10V charge pump circuit
Wordline decoder circuit
Flash memory cell
15
VG
36
18d
-10V charge pump circuit
Vs
18e
5V charge pump circuit
Source decoder circuit
37

FIG. 3A

40

Table: Voltages For Processing Flash Device

	Vg	Vd	Vs
Program	10	6	0
Erase	-10	0	float
Read	5	1	0

Fig. 3B

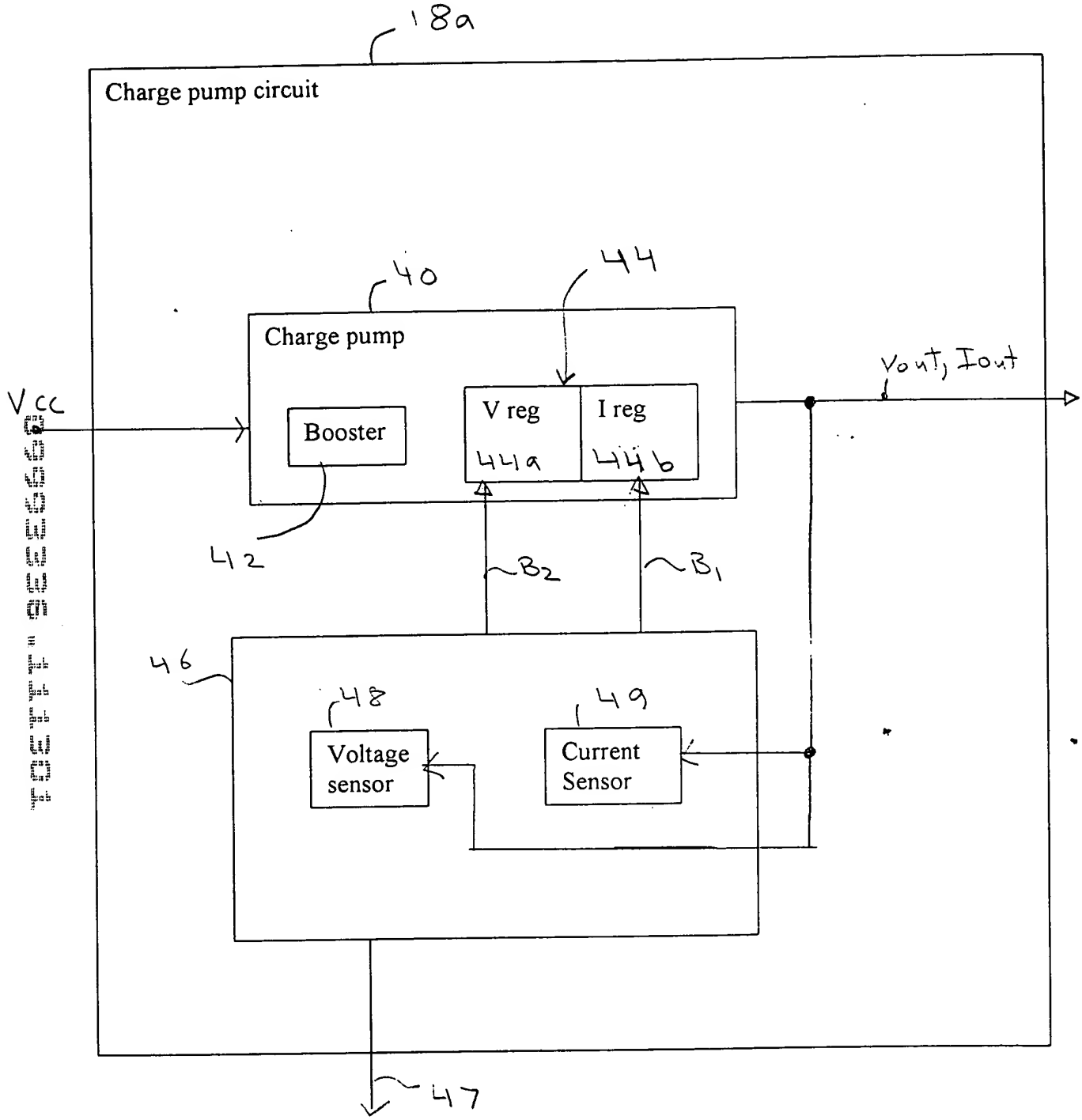
18a
Charge pump circuit
40
44
Charge pump
Vout, Iout
Vcc
Booster
V reg
I reg
44a
44b
42
B2
B1
46
48
49
Voltage sensor
Current Sensor
47

FIG. 4

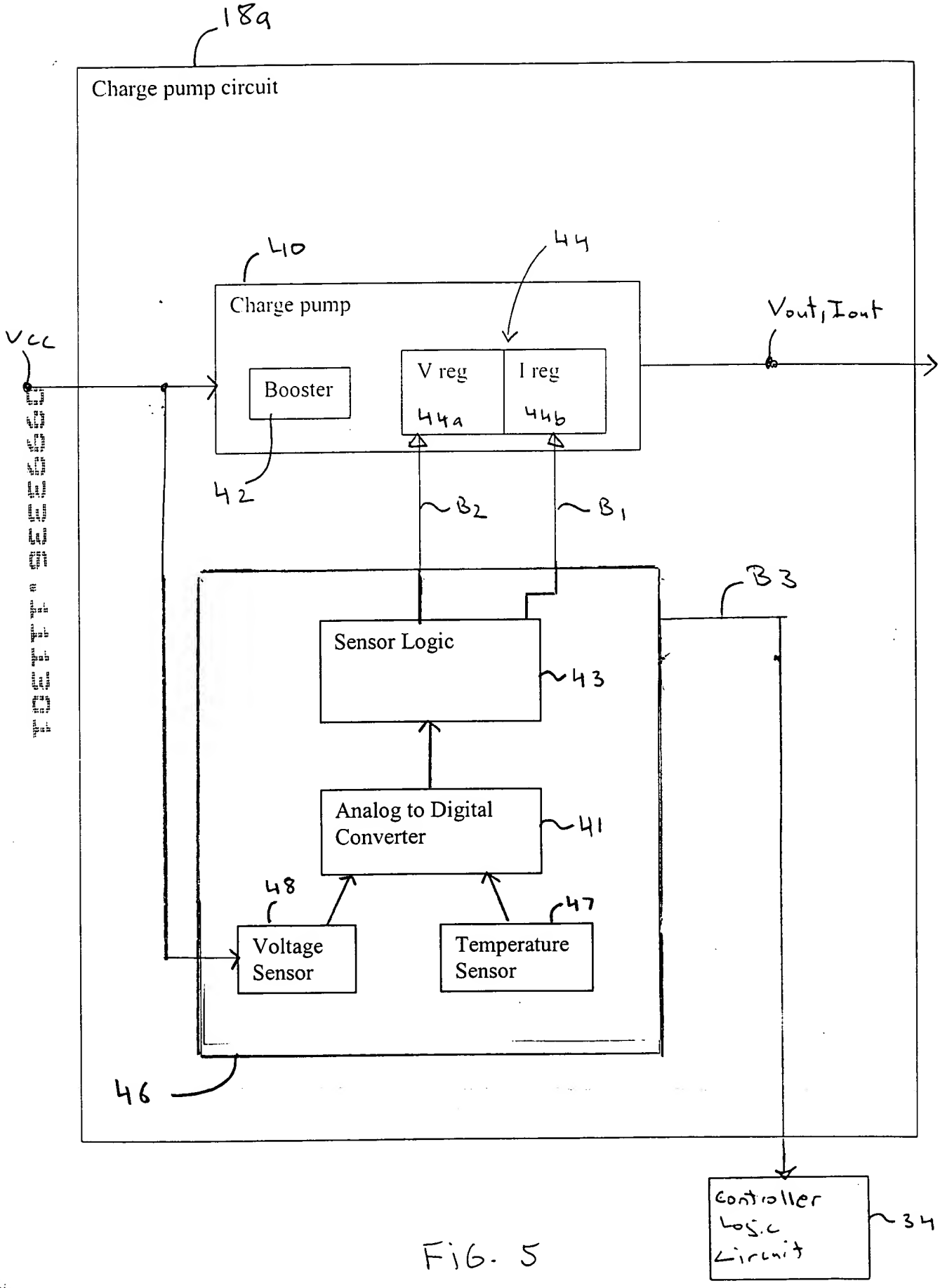
18a
Charge pump circuit
40
Charge pump
44
Booster
V reg
I reg
44a
44b
Vout, Iout
Vcc
42
B2
B1
B3
Sensor Logic
43
Analog to Digital Converter
41
48
47
Voltage Sensor
Temperature Sensor
46
Controller Logic Circuit
34

Fig. 5

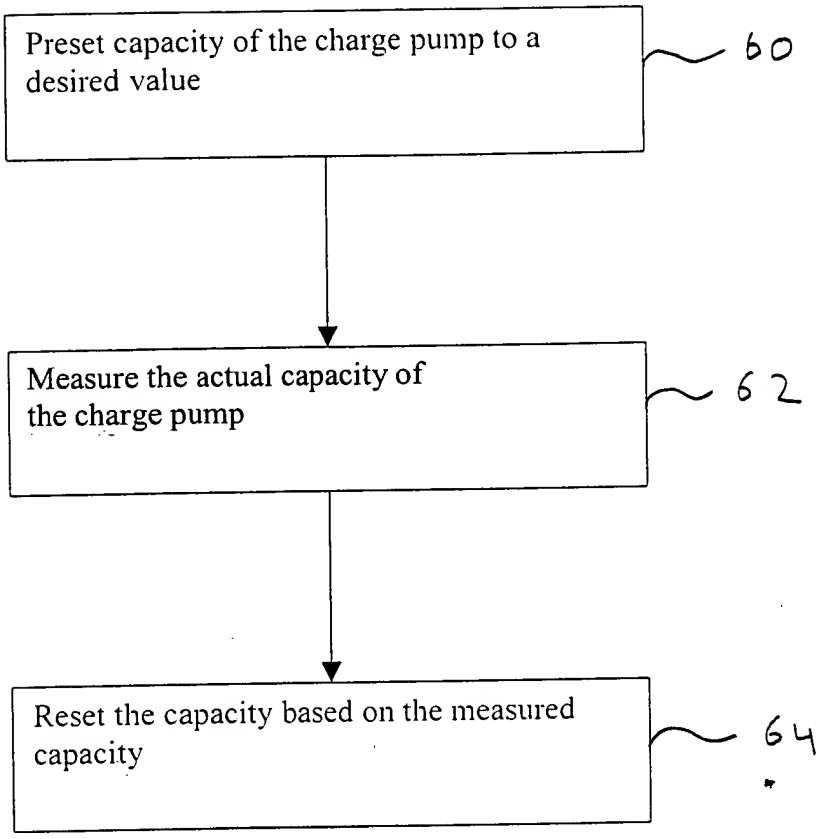
Preset capacity of the charge pump to a desired value
60
Measure the actual capacity of the charge pump
62
Reset the capacity based on the measured capacity
64

FIG. 6